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**CLAIMS:**

What is claimed is:

1. A method for preventing machine crashes due to hard  
5 errors in one of a plurality of processors in a logically  
partitioned data processing system, said method  
comprising the steps of:  
detecting an error in one of said plurality of  
processors;  
10 determining whether said one of said plurality of  
processors has been deconfigured; and  
rebooting configured ones of said plurality of  
processors only in response to a determination that said  
one of said plurality of processors has been  
15 deconfigured.
2. The method according to claim 1, further comprising  
the step of in response to said detecting an error,  
requesting deconfiguration of said one of said plurality  
20 of processors.
3. The method according to claim 1, further comprising  
the step of in response to said one of said plurality of  
processors being deconfigured, providing an indication  
25 that said one of said plurality of processors has been  
deconfigured.
4. The method according to claim 1, further comprising  
the steps of:  
30 providing an exception handler routine;  
detecting, utilizing said exception handler routine,  
said error in said one of said plurality of processors;

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determining, utilizing said exception handler routine, whether said one of said plurality of processors has been deconfigured; and

requesting, utilizing said exception handler  
5 routine, a reboot of said configured ones of said plurality of processors.

5. The method according to claim 4, further comprising the step of requesting, utilizing said exception handler  
10 routine, said one of said processors be deconfigured.

6. The method according to claim 1, further comprising the steps of:

receiving a request to deconfigure said one of said  
15 plurality of processors;

deconfiguring said one of said plurality of processors; and

storing an indication of deconfiguration in response to a completion of deconfiguring said one of said  
20 plurality of processors.

7. The method according to claim 6, further comprising the step of storing said indication in non-volatile  
25 memory.

8. The method according to claim 1, further comprising the steps of:

providing a service processor within said logically partitioned data processing system;

30 in response to said detecting an error,  
deconfiguring said one of said plurality of processors utilizing said service processor; and

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providing, utilizing said service processor, an indication that said one of said plurality of processors has been deconfigured.

5 9. The method according to claim 1, wherein the step of detecting an error in one of said plurality of processors further comprises the step of detecting a hard error in one of said plurality of processors.

10 10. The method according to claim 1, wherein the step of detecting an error in one of said plurality of processors further comprises the step of detecting an address translation error in one of said plurality of processors.

15 11. The method according to claim 1, wherein the step of detecting an error in one of said plurality of processors further comprises the step of detecting a translation look aside buffer address translation error in one of said plurality of processors.

20 12. The method according to claim 1, wherein the step of detecting an error in one of said plurality of processors further comprises the step of detecting a data effective to real address translation error in one of said  
25 plurality of processors.

13. A method for preventing machine crashes due to hard errors in one of a plurality of processors in a logically partitioned data processing system, said method  
30 comprising the steps of:  
providing an error handler routine;

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providing a service processor within said logically partitioned data processing system;

detecting, utilizing said error handler routine, an error in one of said plurality of processors;

5 in response to said error handler routine detecting an error, requesting, utilizing said error handler routine, said service processor to deconfigure said one of said plurality of processors;

10 deconfiguring, utilizing said service processor, said one of said plurality of processors;

in response to a completion of said deconfiguration of said one of said plurality of processors, storing, utilizing said service processor, an indication in a non-volatile memory that said one of said plurality of  
15 processors has been deconfigured;

determining, utilizing said error handler routine, whether an indication has been stored in said non-volatile memory indicating that said one of said plurality of processors has been deconfigured;

20 only in response to a determination that said indication has been stored in said non-volatile memory that said one of said plurality of processors has been deconfigured, requesting, utilizing said error handler routine, a reboot of configured ones of said plurality of  
25 processors; and

rebooting, utilizing said service processor, said configured ones of said plurality of processors.

14. A logically partitioned data processing system for  
30 preventing machine crashes due to hard errors in one of a plurality of processors included in said logically partitioned data processing system, comprising:

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means for detecting an error in one of said plurality of processors;

means for determining whether said one of said plurality of processors has been deconfigured; and

5 means for rebooting configured ones of said plurality of processors only in response to a determination that said one of said plurality of processors has been deconfigured.

10 15. The system according to claim 14, further comprising in response to said detecting an error, means for requesting deconfiguration of said one of said plurality of processors.

15 16. The system according to claim 14, further comprising in response to said one of said plurality of processors being deconfigured, means for providing an indication that said one of said plurality of processors has been deconfigured.

20 17. The system according to claim 14, further comprising:

an exception handler routine;

25 said exception handler routine for detecting said error in said one of said plurality of processors;

said exception handler routine for determining whether said one of said plurality of processors has been deconfigured; and

30 said exception handler routine for requesting a reboot of said configured ones of said plurality of processors.

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18. The system according to claim 17, further comprising said exception handler routine for requesting said one of said processors be deconfigured.

5 19. The system according to claim 14, further comprising:

means for receiving a request to deconfigure said one of said plurality of processors;

10 means for deconfiguring said one of said plurality of processors; and

means for storing an indication of deconfiguration in response to a completion of deconfiguring said one of said plurality of processors.

15 20. The system according to claim 19, further comprising a non-volatile memory for storing said indication.

21. The system according to claim 14, further comprising:

20 a service processor within said logically partitioned data processing system;

in response to said detecting an error, said service processor for deconfiguring said one of said plurality of processors; and

25 said service processor for providing an indication that said one of said plurality of processors has been deconfigured.

30 22. The system according to claim 14, wherein said means for detecting an error in one of said plurality of processors further comprises means for detecting a hard error in one of said plurality of processors.

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23. The system according to claim 14, wherein said means  
for detecting an error in one of said plurality of  
processors further comprises means for detecting an  
address translation error in one of said plurality of  
5 processors.

24. The system according to claim 14, wherein said means  
for detecting an error in one of said plurality of  
processors further comprises means for detecting a  
10 translation look aside buffer address translation error  
in one of said plurality of processors.

25. The system according to claim 14, wherein said means  
for detecting an error in one of said plurality of  
15 processors further comprises means for detecting a data  
effective to real address translation error in one of  
said plurality of processors.

26. A system for preventing machine crashes due to hard  
20 errors in one of a plurality of processors in a  
logically partitioned data processing system, said system  
comprising:

an error handler routine;  
a service processor within said logically  
25 partitioned data processing system;  
said error handler routine for detecting an error in  
one of said plurality of processors;  
in response to said error handler routine detecting  
an error, said exception handler routine for requesting  
30 said service processor to deconfigure said one of said  
plurality of processors;

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said service processor for deconfiguring said one of said plurality of processors;

in response to a completion of said deconfiguration of said one of said plurality of processors, said service processor for storing an indication in a non-volatile memory that said one of said plurality of processors has been deconfigured;

said error handler routine for determining whether an indication has been stored in said non-volatile memory indicating that said one of said plurality of processors has been deconfigured;

only in response to a determination that said indication has been stored in said non-volatile memory that said one of said plurality of processors has been deconfigured, said exception handler routine for requesting a reboot of configured ones of said plurality of processors; and

said service processor for rebooting said configured ones of said plurality of processors.

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27. A computer program product for preventing machine crashes due to hard errors in one of a plurality of processors in a logically partitioned data processing system, said computer program product comprising:

instruction means for detecting an error in one of said plurality of processors;

instruction means for determining whether said one of said plurality of processors has been deconfigured; and

instruction means for rebooting configured ones of said plurality of processors only in response to a

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determination that said one of said plurality of processors has been deconfigured.

28. The product according to claim 27, further  
5 comprising in response to said detecting an error, instruction means for requesting deconfiguration of said one of said plurality of processors.

29. The product according to claim 27, further  
10 comprising in response to said one of said plurality of processors being deconfigured, instruction means for providing an indication that said one of said plurality of processors has been deconfigured.

30. The product according to claim 27, further  
15 comprising:  
instruction means for providing an exception handler routine;

instruction means for detecting, utilizing said  
20 exception handler routine, said error in said one of said plurality of processors;

instruction means for determining, utilizing said  
exception handler routine, whether said one of said  
plurality of processors has been deconfigured; and

25 instruction means for requesting, utilizing said exception handler routine, a reboot of said configured ones of said plurality of processors.

31. The product according to claim 30, further  
30 comprising instruction means for requesting, utilizing said exception handler routine, said one of said processors be deconfigured.

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32. The product according to claim 27, further comprising:

instruction means for receiving a request to deconfigure said one of said plurality of processors;

5 instruction means for deconfiguring said one of said plurality of processors; and

instruction means for storing an indication of deconfiguration in response to a completion of deconfiguring said one of said plurality of processors.

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33. The product according to claim 32, further comprising instruction means for storing said indication in non-volatile memory.

15 34. The product according to claim 27, further comprising:

instruction means for providing a service processor within said logically partitioned data processing system;

20 in response to said detecting an error, instruction means for deconfiguring said one of said plurality of processors utilizing said service processor; and

instruction means for providing, utilizing said service processor, an indication that said one of said plurality of processors has been deconfigured.

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35. The product according to claim 27, wherein said instruction means for detecting an error in one of said plurality of processors further comprises instruction means for detecting a hard error in one of said plurality  
30 of processors.

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36. The product according to claim 27, wherein said instruction means for detecting an error in one of said plurality of processors further comprises instruction means for detecting an address translation error in one  
5 of said plurality of processors.

37. The product according to claim 27, wherein said instruction means for detecting an error in one of said plurality of processors further comprises instruction  
10 means for detecting a translation look aside buffer address translation error in one of said plurality of processors.

38. The product according to claim 27, wherein said  
15 instruction means for detecting an error in one of said plurality of processors further comprises instruction means for detecting a data effective to real address translation error in one of said plurality of processors.

39. A computer program product for preventing machine  
20 crashes due to hard errors in one of a plurality of processors in a logically partitioned data processing system, said computer program product comprising:

instruction means for providing an error handler  
25 routine;

instruction means for providing a service processor within said logically partitioned data processing system;

instruction means for detecting, utilizing said error handler routine, an error in one of said plurality  
30 of processors;

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in response to said error handler routine detecting an error, instruction means for requesting, utilizing said error handler routine, said service processor to deconfigure said one of said plurality of processors;

5 instruction means for deconfiguring, utilizing said service processor, said one of said plurality of processors;

in response to a completion of said deconfiguration of said one of said plurality of processors, instruction  
10 means for storing, utilizing said service processor, an indication in a non-volatile memory that said one of said plurality of processors has been deconfigured;

instruction means for determining, utilizing said error handler routine, whether an indication has been  
15 stored in said non-volatile memory indicating that said one of said plurality of processors has been deconfigured;

only in response to a determination that said indication has been stored in said non-volatile memory  
20 that said one of said plurality of processors has been deconfigured, instruction means for requesting, utilizing said error handler routine, a reboot of configured ones of said plurality of processors; and

instruction means for rebooting, utilizing said  
25 service processor, said configured ones of said plurality of processors.